

RAM KRISHNA DEWANGAN



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ACADEMIC PROFILE

S.No.	Name of Exam	Discipline/ Specialization	Name of Institute/ Board/ University	Passing year	Percentage/ CPI
1.	M. Tech.	VLSI Design	Nirma University, Ahmedabad	May 2009	CPI- 8.01/10
2.	B.E.	ECE	ITGGU, Bilaspur	June 2006	72.20%
3.	AISSCE	PCM	J.N.V. Mana, Raipur, CBSE Board	June 2002	75.2%
4.	AISSE	Common	J.N.V. Mana, Raipur, CBSE Board	June 2000	75.6%

➤ Qualified GATE 2007 Exam with 94.0 percentile.

SUBJECT OF INTEREST

1. VLSI Design & VHDL
2. Analog Circuit Design
3. Digital Electronics
4. Microprocessor & Microcontrollers
5. Automatic Control System

PAPER PRESENTATION/ PUBLICATION & SEMINARS

PUBLICATION IN INTERNATIONAL JOURNALS	
1.	Implementation of High Performance QDR-II SRAM Interface with Xilinx FPGA (ICACEEE- 2012)
2.	Design of RF CMOS Mixer at 30 MHz using 0.12 micron Technology (ICACEEE- 2012)

NATIONAL CONFERENCE

1	High Performance QDR-II SRAM and DDR-II SDRAM Interface with Xilinx FPGA (NATCON- 2012)
2	Design of high speed 32x32 bit multiplier using Booth- Wallace Algorithm (NATCON- 2012)
3	Design of multi baud rate Universal Asynchronous Receiver Transmitter with FIFO (TECHNOLOGIA- 2012)
SEMINAR/ WORKSHOP ATTENDED	
1	“National Seminar on Nanotechnology” organized by Nirma University on January 19th, 2009.
2	Workshop on “Advance EDA tools for VLSI Testing” organized by Nirma University on March 27-28th , 2009.
3	“National Conference on current Trends in Technology” organized by Nirma University (NUCONE-2007, NUCONE-2008)

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